**Introduction to SystemVerilog HDVL**

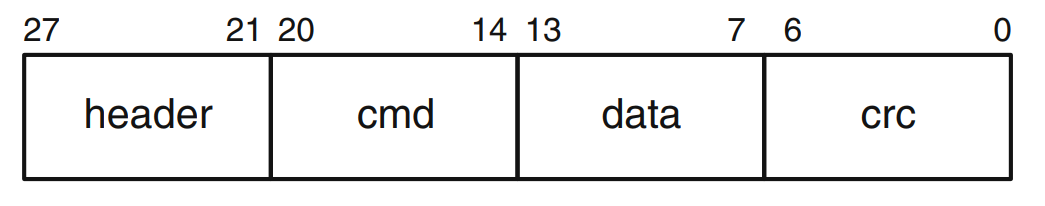
**Lab Manual**

**Lab 1: SystemVerilog Packed Structures**

**Objective: *The objective of this lab is to get introduced to***

* **SystemVerilog Packed and Unpacked structures.**

Define a packed structure for the following packet format shown in Fig 1. Assume header and cmd of 4 state data types, data and crc to be of 2 state data types and initialize them with some value. Access them individually and as a group within an initial block.



**Fig 1: Packet Format**

* **Perform Simulation using Questa- Intel FPGA Starter edition.**

**Lab 2: Dynamic Arrays**

**Objective: *The objective of this lab is to get introduced to***

* **SystemVerilog Dynamic Arrays**

Declare a dynamic array with 30 locations. The contents of the dynamic array should be of random values. Copy the contents of this dynamic array to another dynamic array which has 60 locations in which the first 30 locations should be the same as the original dynamic array. Print contents of both.

* **Perform Simulation using Questa- Intel FPGA Starter edition.**

**Lab 3: Queues**

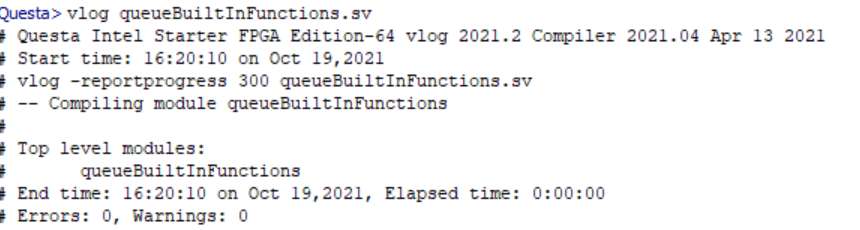
**Objective: *The objective of this lab is to get introduced to***

* **SystemVerilog Queues**

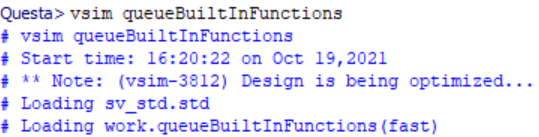
The queueBuiltInFunctions.sv file is provided in the lab3 folder. The built-in functions of the queue have been demonstrated in the code. Explore the usage of size, insert and delete functions in the queue data-structure.

* **Perform Simulation using Questa- Intel FPGA Starter edition.**

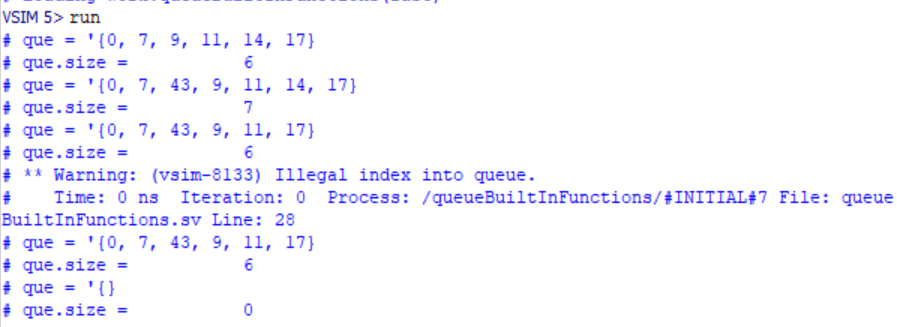
**Compile the given SV file**



**Simulate the module**



**Run**



**END OF LAB EXERCISE**